

CLAIMS

We claim:

1. A GaN based enhancement mode MOSFET, comprising:
 - a GaN comprising layer;
 - a (Group III)_xGa_{1-x}N layer, where x is from 0 to 1, disposed on said GaN layer, a thickness of said (Group III)_xGa_{1-x}N layer being less than 20 nm;
 - a source and a drain extending through said (Group III)_xGa_{1-x}N layer into said GaN layer, said source and drain separated by a channel region,
 - a gate dielectric layer disposed over said channel region, and
 - a gate electrode disposed on said gate dielectric, wherein said MOSFET is in an off-state when said gate is not biased.
2. The transistor of claim 1, wherein said Group III element comprises Al.
3. The transistor of claim 1, wherein x is from 0.2 to 0.35.
4. The transistor of claim 1, wherein said Group III element comprises B.
5. The transistor of claim 1, wherein MOSFET is an n-channel MOSFET.
6. The transistor of claim 1, wherein MOSFET is a p-channel MOSFET.

7. The transistor of claim 1, wherein said $(\text{Group III})_x\text{Ga}_{1-x}\text{N}$ layer is undoped.
8. The transistor of claim 1, wherein said $(\text{Group III})_x\text{Ga}_{1-x}\text{N}$ layer is p-doped.
9. The transistor of claim 1, wherein said thickness of said $(\text{Group III})_x\text{Ga}_{1-x}\text{N}$ layer is less than 10 nm thick.
10. The transistor of claim 1, wherein said thickness of said $(\text{Group III})_x\text{Ga}_{1-x}\text{N}$ layer is less than 5 nm thick.
11. The transistor of claim 1, wherein said thickness of said $(\text{Group III})_x\text{Ga}_{1-x}\text{N}$ layer is 1 to 4 nm thick.
12. The transistor of claim 1, wherein said GaN comprising layer is selected from the group consisting of p-GaN, undoped GaN and InGaN.
13. The transistor of claim 1, further comprising a p-AlGaN or undoped AlGaN layer disposed below said GaN comprising layer.
14. The transistor of claim 1, wherein said gate dielectric layer comprises SiN_x , MgO or Sc_2O_3 .